

DESIGN OF LOW CONVERSION LOSSES COLD FET MIXERS BY STATISTICAL OPTIMIZATION OF HIGH ORDER SIDEBANDS LOADING

J.F. VILLEMAZET* - M. CAMIADE* - J. OBREGON**

* THOMSON-CSF TCS, BP. 46, Route Départementale 128 - 91401 Orsay Cedex - FRANCE
 ** IRCOM-CNRS - Université de Limoges - 123 Av. Albert Thomas - 87060 Limoges - FRANCE

ABSTRACT

This paper proposes a new statistical approach allowing to define design rules of low conversion losses cold FET mixers. Applying these rules, an experimental mixer gives 4 dB intrinsic conversion losses at 7.5 GHz LO frequency with 10.5 dBm power and 10 MHz IF frequency.

INTRODUCTION

Generally, mixers designs are performed by considering only RF, IF and Image terminations. But in a recent paper, Miltra and Maas [1] have shown that using a short circuit embedding impedances at the second and third LO harmonics and their associated mixing frequencies, the diode mixer intermodulation distortion can be improved. In the same way, low conversion losses may be obtained in resistive mixers by suitably loading high order sidebands.

The objective of the proposed method is not to find the accurate optimum load at each mixing frequency to obtain the minimum of conversion losses (probably the resulting values would not be realizable with a practical network). The goal of the proposed design method is to find the correlation existing between loads at the different mixing frequencies allowing to improve the conversion. Once the statistical correlations are found between loads from numerous cases giving low losses, design rules may be defined to synthesize the associated embedding network, to obtain low conversion losses which can be reproduced.

THE STATISTICAL APPROACH

1 - Definitions

Figure 1 shows the large-small signal representation of the mixer. The LO voltage, applied to the gate modulates the cold FET channel conductance at the LO frequency. The RF signal input and the IF extraction are made at the drain port. The conversion losses are computed using the conversion matrix method. To simplify the notation, the notion of "embedding vector" will be associated afterwards to the set of embedding impedances at all the considered mixing frequencies. All the following results will be presented considering $f_{RF} < f_{LO}$.

Figure 2 presents the I/V characteristics of the used 4 x 75 μ m low power GaAs FET. The current model is :

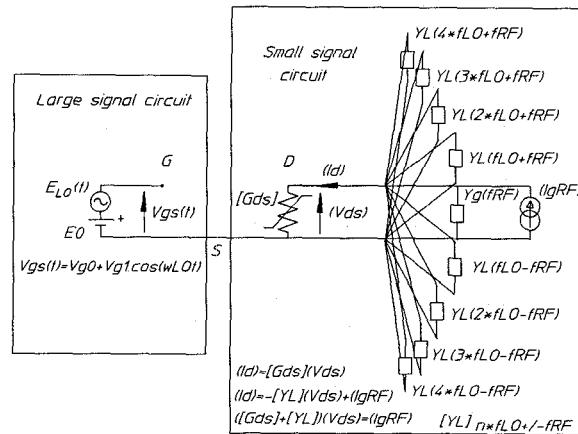


Fig-1 - Large-small signal representation of the mixer

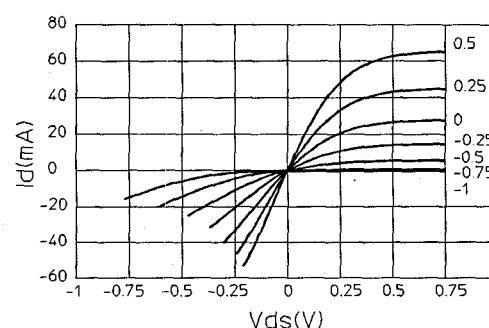
$$Id(Vgs, Vds) = Idss \left(1 + \frac{Vgeff}{Vt} \right)^n \tanh(\alpha Vds)$$

with if $Vgs \geq Vgd$.

$$Vgeff = \frac{1}{2} \left[\sqrt{(Vgs - Vt)^2 + \Delta^2} - \sqrt{(Vgd - Vb)^2 + \Delta^2} \right] + \frac{Vt + Vb}{2}$$

and if $Vgs < Vgd$

$$Vgeff = \frac{1}{2} \left[\sqrt{(Vgd - Vt)^2 + \Delta^2} - \sqrt{(Vgd - Vb)^2 + \Delta^2} \right] + \frac{Vt + Vb}{2}$$



OF2

Fig-2 - I/V characteristics of the used GaAs FET for Vgs from 0.5 V to -1V

2 - The statistical approach

The aim is to extract trends on embedding impedances from numerous cases corresponding to minimum losses and subsequently to verify that these properties are sufficient to improve the conversion in all cases.

To perform this, the first step is to generate a representative population of embedding vectors. A software has been developed to compute an uniform random sequence for each element of the embedding vectors. The real part values of the generated impedances are limited from 0 to 500Ω , the imaginary part from -500 to 500Ω , which represents a realizable impedance range. The conversion losses are then computed and a first statistic is made by counting the number of vectors for different losses classes. Figure 3 presents, in percentage, the losses population repartition from 0 to 20 dB per 0.5 dB classes. For the chosen nonlinear device, the chosen LO voltage and the chosen impedances range, the statistic shows that there is quite no chance to have losses smaller than 3.5 dB. On the other hand, the probability to obtain losses near 7 dB is highest as we can observe in reality.

The embedding vectors allowing the best losses, under 4.5 dB, are then selected to make a new population of optimum vectors. Figure 3 shows that such vectors represent 1 % of the initial population. A new statistic on this optimum population displays the embedding impedances repartition at each mixing frequency. Figure 4 (abc) leads to three loading behaviours as a function of these frequencies :

1. The first, Figure 4a concerns the RF and IF embedding impedances. They have the same statistical repartition which corresponds to a purely resistive impedance.

2. The second kind, Figure 4b concerns the $f_{LO} + f_{RF}$ frequency and the Image frequency $2f_{LO} - f_{RF}$. They have also the same statistical distribution which corresponds, in this case, to purely reactive high impedance.

3. The third and last kind, Figure 4c, concerns the $2f_{LO} + f_{RF}$ frequency which is also representative of the other higher mixing frequencies. Figure 4c shows that here isn't a clear trend other than a poor one corresponding to a small resistive part. But above all, the Figure 4c repartition looks like an uniform probability density function that is to say, whatever the impedance values, the losses are minimum. So, the embedding impedances at $2f_{LO} + f_{RF}$ frequency and higher mixing frequencies don't have an important part in the conversion losses calculation.

Other correlations between some mixing frequencies embedding impedances can appear. Even if RF and IF terminations are mainly resistive near the optimum, they can have however a small reactance. The population distribution of this reactance is a Gaussian function (Figure 4a). In figure 5a, a statistic gives again the RF reactance repartition but the optimum population has been divided in two parts according to the RF reactance sign. Figure 5b shows consequently the reactance distribution of the $f_{LO} + f_{RF}$ frequency with the same division between vectors which have positive or negative RF reactances. There is now an inversion of the two separate population : the optimum vector with a positive RF reactance,

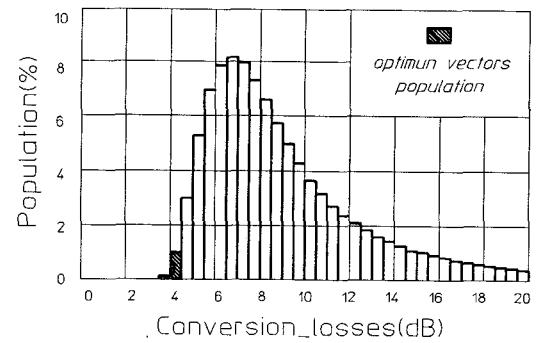


Fig. 3 - Statistical repartition of conversion losses computed from 500 000 random embedding vectors

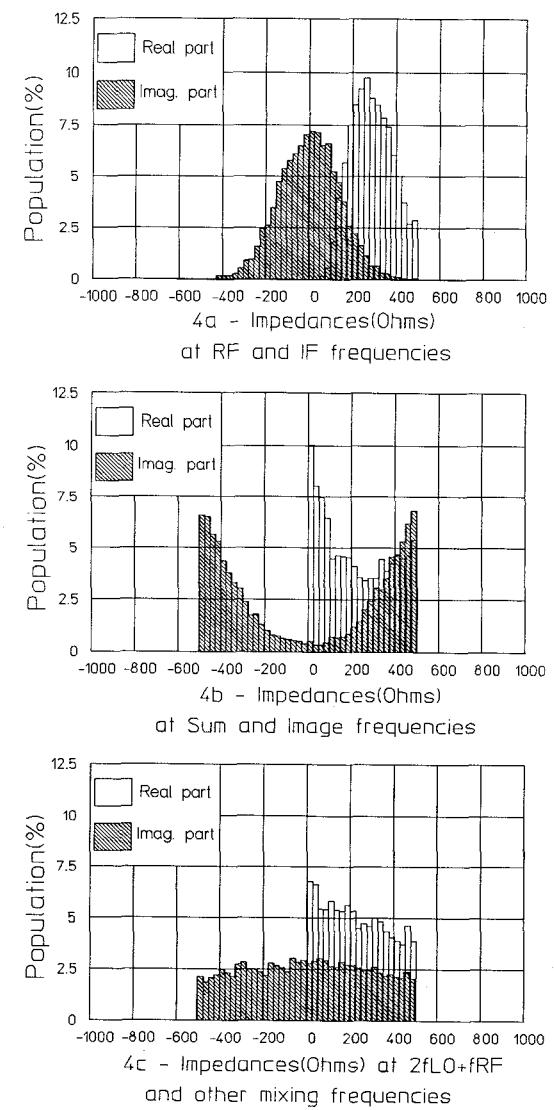


Fig.4 . Statistical repartition of the embedding impedances from the optimum vectors population (giving losses smaller than 4.5 dB)

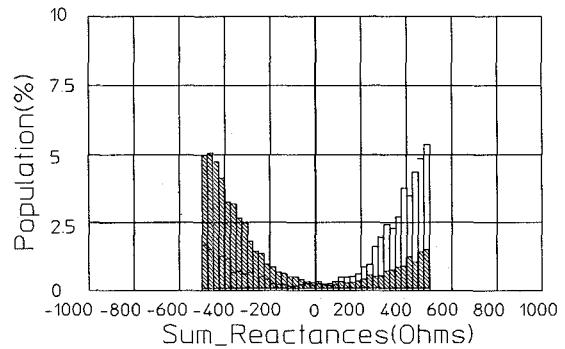
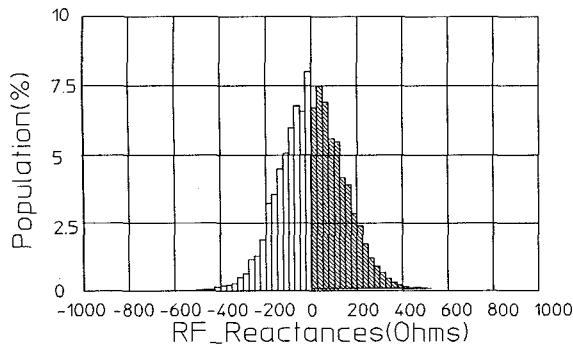


Fig-5 . RF and Sum frequencies reactances repartition. The population is divided as a function of RF reactance sign

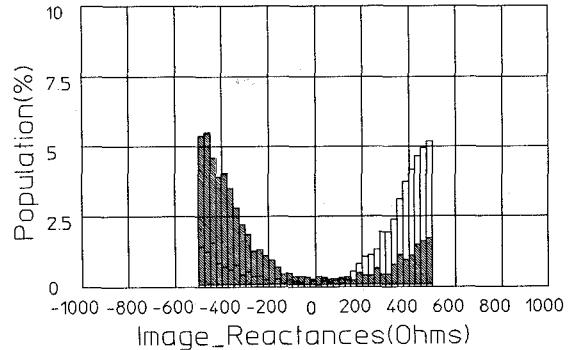
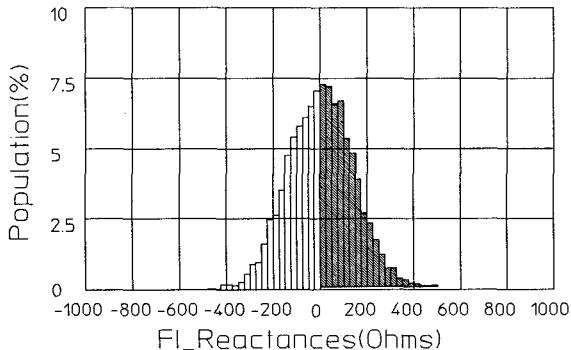


Fig-6 .- IF and Image frequencies reactances repartition. The population is divided as a function of IF reactance sign

have a negative $f_{LO} + f_{RF}$ reactance and vice versa. Using the same approach, figures 6a, 6b show that the optimum vectors which have positive IF reactances, have negative Image reactances and vice versa.

MAIN RESULTS AND DESIGN RULES

The most important frequencies in the conversion calculation are not only the RF, IF, Image frequencies but also the $f_{LO} + f_{RF}$ the Sum frequency. This frequency is always located near the second LO harmonic in down converter mixers.

The optimal embedding configuration is then :

- a resistive finite impedance for RF and IF frequencies
- a high impedance that is to say an open circuit for Sum and Image frequencies.

This configuration is confirmed by using a Gradient optimization. This algorithm always converges to high Sum and Image impedances.

Pratically, it may be difficult to achieve open circuits at Sum and Image frequencies. So using the results of the previous statistics (figure 4), an other embedding configuration, corresponding to a limited available impedance range, can be proposed :

$$\begin{aligned}
 Z_{RF} &= R_{RF} + j X_{RF} \quad \text{with } R_{RF} \approx R_{IF} \\
 Z_{IF} &= R_{IF} + j X_{IF} \\
 Z_{Sum} &= j X_{Sum} \quad \text{with } X_{Sum} \text{ and } X_{Image} \text{ highest} \\
 Z_{Image} &= j X_{Image} \quad \text{values in the impedance range}
 \end{aligned}$$

with the jX opposition rule :

$$\begin{aligned}
 \text{sign}(X_{Sum}) &= - \text{sign}(X_{RF}) & \text{(figures 5 and 6)} \\
 \text{sign}(X_{Image}) &= - \text{sign}(X_{IF})
 \end{aligned}$$

As the previous ideal configuration, the aim is to avoid the power dissipation at the Sum and Image frequencies, but in this case, this condition leads to non resistive impedances. Furthermore, Saleh [2] has proved that the optimum passive embedding network for a mixer with a non negative time-varying resistance is lossless ; i.e., the out-of-band frequencies should be terminated reactively. In this case, the nonlinearity generates powers at Sum and Image frequencies but these are reactive powers. Using the jX opposition rule, it is possible to use a part of these powers to improve the conversion at the IF frequency, giving rise to Image recovery mixers.

To validate the rule, Figures 7a, 7b has been drawn to compare the conversion losses statistics between a random embedding impedances population and a population with reactive terminations at Sum and Image frequencies, and satisfying the jX opposition propertie. So using the jX opposition rule, the probability to obtain low conversion losses is clearly increased. Finally to show the importance of this rule, figures 7a, 7c give the comparison between a random population and a population with reactive terminations at Sum and Image frequencies too, but satisfying the contrary of the jX opposition propertie.

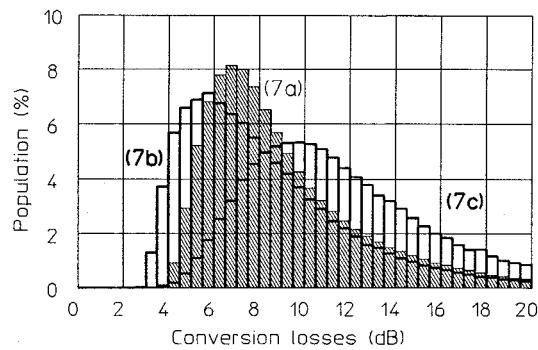


Fig-7 . Statistical repartition of conversion losses computed from (a) a random population, (b) a population satisfying the jX rule and (c) a population satisfying the contrary of the rule

EXPERIMENTAL RESULTS

The circuit shown in the figure 8 realizes a LO matching on the gate port of the cold FET and the classical RF/IF diplexer on the drain. Furthermore, on the drain, the L_p inductance generates a parallel resonance with the FET capacitance in the FET current source plane. This resonance, tuned at a frequency located between LO and its second harmonic allows to create reactances of opposite signs at the RF and Sum frequencies. The drain network permits to realize the same signs opposition between IF and Image reactances. Figure 9 shows load impedances that such circuit allows to obtain, as a function of the frequency. The elements values have been calculated on a circuit simulator to achieve the set of embedding impedances satisfying the optimal configuration. The circuit has been realized in hybrid technology. The overall circuit has been analyzed as a mixer with an harmonic balance simulator. Figures 10a, 10b present a comparison between simulated and measured circuit response. It may be noted that the simulation and the measurement are in a very good agreement. The simulation allows to calculate the intrinsic conversion losses. Figure 10c shows that the external 5 dB experimental minimum corresponds to 4 dB intrinsic conversion losses. It is so verified that the method is very efficient and leads to an embedding configuration giving very low conversion losses.

CONCLUSION

We have developed a new design method based on a statistical approach, which allows to obtain theoretically general design rules for the cold FET mixers embedding networks. These design rules, experimentally verified, lead to low and predictable conversion losses. This last aspect becomes more and more attractive, in particular in MMIC circuits, when high design yield is synonymous of low cost. Now, the method will be used to improve the noise figure and the intermodulation distortion and can also be applied to diode mixers.

This work was supported by DRET (Direction des Recherches Etudes et Techniques) under contract n° 90/470.

REFERENCES

1. S.G. Mitra and S. Maas, "A Diode Mixer with Harmonic-Distortion Suppression". IEEE Microwave and Guided Wave Letters, Vol. 2, 1992, p 417.
2. Adel A. M. Saleh, "Theory of Resistive Mixers". Research Monograph # 64, 1971, The Massachusetts Institute of Technology.

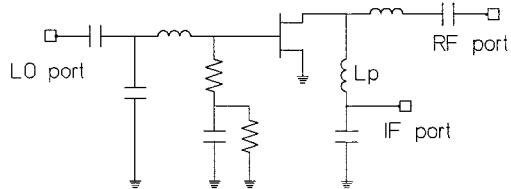


Fig-8 . Cold FET mixer circuit

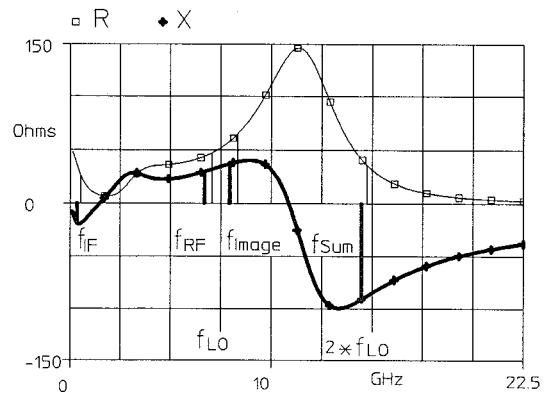


Fig-9 . $R + jX$ load synthesized by the circuit on the FET drain. The jX opposition rule is verified

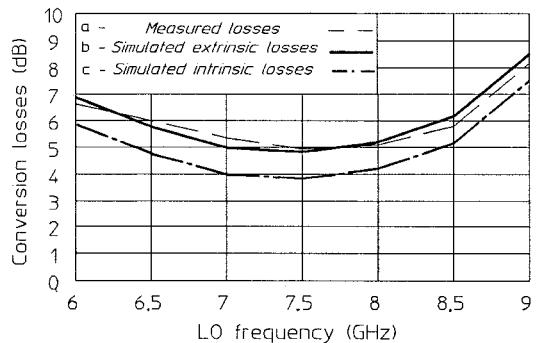


Fig-10 . (a) Measured circuit conversion losses, (b) simulated losses and (c) corresponding intrinsic losses.